AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) ~~The~~ A liquid crystal display of horizontal electric field applying type comprising:

a thin film transistor array substrate, wherein the thin film transistor array substrate includes an effective display area having a gate line, a common line parallel to the gate line, a data line ~~intersected~~ crossing and isolated ~~with~~ from the gate line and the common line with a gate insulating film therebetween to define a pixel area, a thin film transistor formed ~~on~~ at each ~~intersection~~ crossing of the gate line and the data line, a passivation film for protecting the thin film transistor, a common electrode formed in the pixel area and connected to the common line, and a pixel electrode connected to the thin film transistor and formed to produce a horizontal electric field along with the common electrode in the pixel area, and a pad area having a gate pad formed ~~with~~ to have at least one conductive layer included in the gate line, a data pad formed ~~with~~ to have at least one conductive layer included in the data line, and a common pad formed ~~with~~ to have at least one conductive layer included in the common line~~, which are formed on a lower substrate to form the thin film transistor array substrate~~;

a color filter array substrate ~~combined with~~ facing the thin film transistor array substrate ~~as facing each other~~;

a driving integrated circuit mounted on the thin film transistor substrate ~~in order~~ to directly connect to ~~any~~ one of the gate pad and the data pad; and

a package mold material for capsulating the pads and the driving integrated circuit.

2. (Currently Amended) The liquid crystal display of horizontal electric field applying type according to claim 1, wherein the passivation film is formed on the effective display area except for the pad area ~~region~~.

3. (Original) The liquid crystal display of horizontal electric field applying type according to claim 1, wherein the driving integrated circuit includes a gate driving integrated circuit connected to the gate pad.

4. (Original) The liquid crystal display of horizontal electric field applying type according to claim 3, wherein the driving integrated circuit further includes a data driving integrated circuit connected to the data pad.

5. (Original) The liquid crystal display of horizontal electric field applying type according to claim 1, further comprising a plurality of signal supplying lines for supplying a driving signal to the driving integrated circuit.

6. (Original) The liquid crystal display of horizontal electric field applying type according to claim 5, further comprising a connector to which a conductive film for supplying a driving signal to the signal supplying line is attached.

7. (Original) The liquid crystal display of horizontal electric field applying type according to claim 6, further comprising a second package mold material for capsulating a boundary portion of the connector and the conductive film and a boundary portion of the lower substrate and the conductive film.

8. (Original) The liquid crystal display of horizontal electric field applying type according to claim 1, wherein each of the gate line and the common line includes a main conductive layer and a subsidiary conductive layer for providing against an opening of the main conductive layer.

9. (Original) The liquid crystal display of horizontal electric field applying type according to claim 8, wherein each of the gate pad and the common pad includes the main conductive layer and the subsidiary conductive layer, and wherein the subsidiary conductive layer has an exposed structure.

10. (Original) The liquid crystal display of horizontal electric field applying type according to claim 8, wherein each of the gate pad and the common pad includes the subsidiary conductive layer.

11. (Currently Amended) The liquid crystal display of horizontal electric field applying type according to claim 1, wherein the data line includes a main conductive layer and a subsidiary conductive layer ~~for providing~~ to protect against ~~the~~ an opening of the main conductive layer.

12. (Original) The liquid crystal display of horizontal electric field applying type according to claim 11, wherein the data pad includes the main conductive layer and the subsidiary conductive layer, and wherein the subsidiary conductive layer has an exposed structure.

13. (Original) The liquid crystal display of horizontal electric field applying type according to claim 11, wherein the data pad includes the subsidiary conductive layer.

14. (Currently Amended) The liquid crystal display of horizontal electric field applying type

according to claim 1, wherein the thin film transistor comprises:

a gate electrode connected to the gate line;

a source electrode connected to the data line;

a drain electrode facing ~~with~~ the source electrode; and

a semiconductor layer ~~overlapped with~~ overlapping the gate electrode with the gate insulating film therebetween to form a channel portion between the source electrode and the drain electrode.

15. (Original) The liquid crystal display of horizontal electric field applying type according to claim 14, wherein the drain electrode and the pixel electrode are made of an identical conductive layer.

16. (Currently Amended) The liquid crystal display of horizontal electric field applying type according to claim 14, wherein the with semiconductor layer is formed on the gate insulating film along the data line, the source electrode, the drain electrode and the pixel electrode.

17. (Currently Amended) A method for fabricating a liquid crystal display of horizontal electric field applying type, comprising ~~which comprises steps of~~:

preparing a thin film transistor array substrate having an effective display area and a pad area formed on a lower substrate, wherein the effective display area includes a gate line, a common line parallel to the gate line, a data line ~~intersected with~~ crossing the gate line and the common line with a gate insulating film therebetween to define a pixel area, a thin film transistor formed ~~on~~ at each ~~intersection~~ crossing of the gate line and the data line, a passivation for protecting the thin film transistor, a common electrode formed in the pixel area and connected to the common line and a pixel electrode connected to the thin film transistor and formed to

produce horizontal electric field along with the common electrode in the pixel area, and the pad area includes a gate pad formed ~~with~~ having at least one conductive layer included in the gate line, a data pad formed ~~with~~ having at least one conductive layer included in the data line, and a common pad formed ~~with~~ having at least one conductive layer included in the common line;

preparing a color filter array substrate ~~combined with~~ facing the thin film transistor array substrate ~~as facing each other~~;

combining the thin film transistor array substrate and the color filter array substrate to expose the pad area ~~region~~;

exposing the common pad, the gate pad and the data pad;

mounting a driving integrated circuit on the substrate ~~in order~~ to directly connect to ~~any~~ one of the gate pad and the data pad; and

capsulating a pad connected with the driving integrated circuit with a package mold material.

18. (Currently Amended) The method according to claim 17, wherein ~~the step of~~ mounting the driving integrated circuit includes connecting the gate pad and the gate driving integrated circuit.

19. (Currently Amended) The method according to claim 18, wherein ~~the step of~~ mounting the driving integrated circuit further includes connecting the data pad and data driving integrated circuit.

20. (Currently Amended) The method according to claim 17, further comprising ~~the step of~~ forming a plurality of signal supplying lines for supplying a driving signal to the driving integrated circuit.

21. (Currently Amended) The method according to claim 20, further comprising ~~the step of~~ attaching a connector ~~connected~~ to the signal supplying lines with a conductive film ~~for supplying~~ to supply a driving signal to the signal supplying lines.

22. (Currently Amended) The method according to claim 21, further comprising ~~the step of~~ capsulating a boundary portion of the connector and the conductive film and a boundary portion of the lower substrate and the conductive film with a second package mold material.

23. (Currently Amended) The method according to claim 17, wherein ~~the step of~~ preparing a thin film transistor array substrate includes:

forming, on the lower substrate, a first conductive pattern group including the gate line, a gate electrode connected to the gate line, the common line parallel to the gate line, the common electrode, the gate pad and the common pad;

forming a gate insulating film on the lower substrate having the first conductive pattern group thereon;

forming a semiconductor layer at a predetermined area on the gate insulating film and a second conductive pattern group having the date line, a source electrode of the thin film transistor connected with the data line, a drain electrode of the thin film transistor being opposite to the source electrode, a pixel electrode connected with the drain electrode and ~~paralleled~~ parallel to the common electrode and the data pad; and

forming a passivation film ~~for covering~~ to cover the second conductive pattern group.

24. (Currently Amended) The method according to claim 23, wherein ~~the step of~~ exposing the gate pad and the data pad includes etching the gate insulating film and the passivation film using the color filter array substrate as ~~the~~ a mask.

25. (Currently Amended) The method according to claim 23, wherein at least one of the first and the second conductive pattern group is formed to have a double-layered structure having a main conductive layer and a subsidiary conductive layer ~~for providing~~ to protect against ~~the~~ an opening of the main conductive layer.

26. (Currently Amended) The method according to claim 25, wherein ~~the step of~~ exposing the gate pad and the data pad includes exposing the subsidiary conductive layers of the gate pad and the common pad and the subsidiary conductive ~~layer~~ layers of the data pad.